ECIO2 Modbus table

8 DI, 8 DO, 8 AI, 6 AO Release 23.9.2011 ver. 00200

domat control system

- **max 27 words may be read out as a whole (i.e. 54 bytes)**
- **first 256 bits can be addressed bitwise (i.e. 1 LSB – 16 MSB)**

Name	Address	Type	Description	Note
module ID LSB	1 LSB	R	module identification lower byte	module ID is 2101hex
module ID MSB	1 MSB	R	module identification upper byte	
firmware	2 LSB 2 MSB	R	NEC processor FW version	2hex
status LSB	3 LSB	R, W RAM	module status lower byte **bit 0** – EEPROM write enable **bit 4** – EEPROM init **bit 5** – calibration offset **bit 6** – calibration span **bit 7** – calibration enable	**EEPROM init** is enabled when the INIT switch was ON at power-up, and switched OFF before bit 4 was set to 1 (indicated by bit 2 in status MSB) **calibration** is enabled when the INIT switch was ON at power-up, and switched OFF before bit 7 was set to 1 (indicated by bit 3 in status MSB) **calibration offset** change bit 7 from 1 to 0 and set bit 5 to 1 **calibration span** change bit 7 from 1 to 0 and set bit 6 to 1
status MSB	3 MSB	R	module status upper byte **bit 0** - 0 normal mode - 1 init mode **bit 1** - 1 at the next EEPROM write attempt all data will be saved to EEPROM - 0 at the next write attempt received data will be written to RAM only **bit 2** – 1 – EEPROM initialised **bit 3** – 1 – calibration enabled **bit 4** - 0 **bit 5** - 1 **bit 6** - 0 **bit 7** - 1	
firmware 2	4 LSB 4 MSB	R	LPC processor (Ethernet interface)	0x01hex

input range for AI1, AI2	5 LSB	R,W EEPROM	**1 …Pt1000** (-50 to 150 °C) (-5000 to 15000), **divide by 100** to get the correct value **2 … voltage 0V … 10 V** (0 to 10000), **divide by 1000** to get the correct value **3 … resistance 0 … 1600 ohm** (0 to 16000), **divide by 10** to get the correct value **4 … current 0 … 20 mA** (0 to 20000), **divide by 1000** to get the correct value (NB. this range applies only for AI1 to AI4, the switch at the respective input must be set to ON.) **5 … resistance 0 – 5000 ohm** (0 to 50000), **divide by 10** to get the correct value.	bit 0 – bit 3… channel 1 bit 4 – bit 7… channel 2
input range for AI3, AI4	5 MSB	R,W EEPROM		bit 0 – bit 3… channel 3 bit 4 – bit 7… channel 4
input range for AI5, AI6	6 LSB	R,W EEPROM		bit 0 – bit 3… channel 5 bit 4 – bit 7… channel 6
input range for AI7, AI8	6 MSB	R,W EEPROM		bit 0 – bit 3… channel 7 bit 4 – bit 7… channel 8
latch state	7 LSB	R,W EEPROM	state to be catched **0** – log. 0 **1** - log. 1	
relay com	7 MSB	R,W EEPROM	**0** – when no communication, relays stay in last state **1** – when no communication, relays are set to **relay state** values	bit 0 is relay 1 … bit 7 is relay 8
relay state	8 LSB	R,W EEPROM	relays go on or off (according to corresponding bits) if there was no communication with module for a given time and in **relay com** the corresponding relay bit is set to 1	bit 0 is relay 1 … bit 7 is relay 8
relay time	8 MSB	R,W EEPROM	time in [s] of no communication which is considered as communication failure	if set to 0, the function is disabled
relay start enable	9 LSB	R,W EEPROM	startup relay behaviour **0** – relays are not commanded **1** – the corresponding relay is set to its **relay start** value after module startup	bit 0 is relay 1 … bit 7 is relay 8
relay start	9 MSB	R,W EEPROM	relay status between power-up and first bus command	bit 0 is relay 1 … bit 7 is relay 8

relay	10 LSB	R, W RAM	commands to control relay outputs (DO1-DO8)	bit 0 is relay 1 … bit 7 is relay 8
latch enable	10 MSB	R,W RAM	latch function enable for each input – if set to **1** the **latched value** bit goes to 0 and stays so until the latched value is detected; after RESET the register is set to 0	reset the **latched value** register bits to 0 by changing the value of **latch enable** bits from 0 to 1 (= disable and enable latching for individual bits)
analogue outputs AO1	11 LSB	R,W RAM	the AO values are ranged 0000hex – 0FFFhex which is (0 dec – 4095dec) 0000hex is for 0V 0FFFhex is for 10V	analogue output channels
	11 MSB	R,W RAM		
analogue outputs AO2	12 LSB	R,W RAM		
	12 MSB	R,W RAM		
analogue outputs AO3	13 LSB	R,W RAM		
	13 MSB	R,W RAM		
analogue outputs AO4	14 LSB	R,W RAM		
	14 MSB	R,W RAM		
analogue outputs AO5	15 LSB	R,W RAM		
	15 MSB	R,W RAM		
analogue outputs AO6	16 LSB	R,W RAM		
	16 MSB	R,W RAM		
inputs	17 LSB	R	readout of binary inputs (DI1-DI8)	bit 0 is input 1 … bit 7 is input 8
latched value	17 MSB	R	catched values **0 –** if since latch enable the latched state has not been detected at the input **1 -** if since latch enable the latched state has been detected at the input	reset of individual bits: disable and enable the corresponding bits – see register **latch enable**
channel value AI1	18 LSB	R	measured values at analogue inputs; scaling: see **input ranges** registers (regs. 5 to 6)	readouts of analogue inputs AI1..AI8
	18 MSB	R		
channel value AI2	19 LSB	R		
	19 MSB	R		
channel value AI3	20 LSB	R		
	20 MSB	R		
channel value AI4	21 LSB	R		
	21 MSB	R		
channel value AI5	22 LSB	R		
	22 MSB	R		
channel value AI6	23 LSB	R		
	23 MSB	R		
channel value AI7	24 LSB	R		
	24 MSB	R		

channel value AI8	25 LSB	R		
	25 MSB	R		
uptime	26 LSB 27 MSB	R	uptime [s]	